DUAL MATCH-LINE, TWIN-CELL, BINARY-TERNARY CAM

Abstract of Disclosure

A content addressable memory (CAM)(10, 102) and method having a data-in sub-circuit (44), memory cells (16, 18), a match-high line (36), a match-low line (38), and pre-charge devices (40, 42). Input lines (30, 32, 48, 50) from the data-in sub-circuit (44) are not necessarily discharged to ground in every cycle of a clock signal (62) used by the memory cells (16, 18). Further, the pre-charge devices (40, 42) may be operated at one half of the rate of the clock signal (62). Yet further, the CAM (10, 102) may be selectively configured to operate in either binary or ternary mode.

Figures